PCD8572

1K (128 X 8) Serial Electrically Erasable PROM

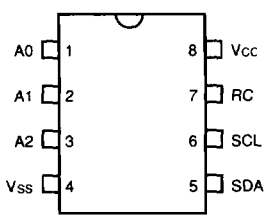
FEATURES

- Organization as 128 bytes (128 x 8)
- Two wire serial interface bus
- 5 volt only operation
- Compatible with the I²C bus
- Fully TTL compatible inputs and outputs
- Unlimited read access
- ESD Protection:
  —Inputs are designed to meet 1.0kV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 read/write cycles per word
- 8-pin DIP package
- Available for extended temperature ranges:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C

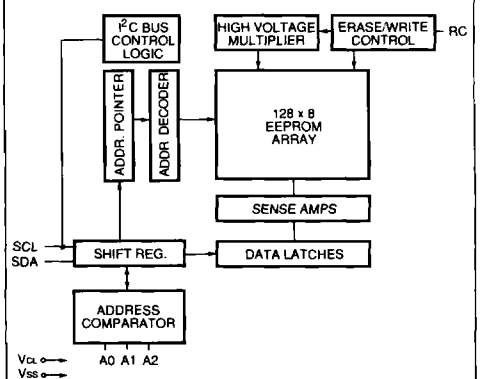
DESCRIPTION

The PCD8572 is a 1K EEPROM manufactured using Microchip Technology's highly reliable SNOS technology. The key features of this device are its +5 volt only operation and inter-integrated circuit (I²C) bus compatibility. This revolutionary bus provides the facilities of a local area network within a single system or equipment. Each IC serves as both transmitter and receiver in the synchronous data transfer of up to 100K bits per second. The use of I²C compatible devices make possible modular circuit design with up to 600 feet of separation allowable between IC's (400pf maximum bus capacitance). Chip select is accomplished by means of the three address inputs A0, A1 and A2. Each of these inputs must be connected externally to either +5V or GND and each chip is then selected through software by placing its 3-bit chip select address on the serial data input line (SDA) at the appropriate time in the bus protocol. Up to eight PCD8572s may be connected to the I²C bus.

PIN CONFIGURATION



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs w.r.t. Vss ..... -0.3V to +7.0V
Voltage on any input pin ..... Vss -0.8 to Vcc +0.8V
Storage temperature (unpowered and without data retention) ..... -65°C to +150°C
Ambient operating temperature with power applied ..... -65°C to +125°C
Current into any input pin ..... 100µa (max.)
Output sink current ..... 3 mA (max.)
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on all pins ..... 1.0kV (typical)

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
A0, A1, A2	Chip address Inputs
Vss	Ground
SDA	Serial Data/Address, Input/Output
SCL	Serial Clock Input
RC	Time Constant Network Input
Vcc	+5V Power Supply

DC CHARACTERISTICS

Vcc = +5V ±10% Vss = 0V (GND)
Commercial (C): Tamb = 0°C to 70°C
Industrial (I): Tamb = -40°C to 85°C

Parameter	Sym	Min	Typ	Max	Units	Conditions
Operating Supply Current READ Mode	ICCR	—	15	—	mA	
Operating Supply Current WRITE/ERASE Mode	ICCW	—	15	—	mA	
Operating supply current STANDBY Mode	ICC0	—	12	—	mA	
Input Leakage Current (A0, A1, A2, SCL Pins)	IIL	—	—	1	µA	
Output Leakage Current HIGH	IOH	—	—	1	µA	
SCL Input and SDA Input/ Output Pins: HIGH Level Input Voltage	VIH	3.0	—	Vcc+0.8	V	
Low Level Input Voltage	VIL	-0.3	—	1.5	V	
Low Level Output Voltage	VOL	—	—	0.4	V	IOL = 3 mA Vcc = 4.5V
A0, A1, A2, Pins: High Level Input Voltage	VIH	Vcc-0.5	—	Vcc+0.5	V	
Low Level Input Voltage	VIL	-0.3	—	0.5	V	

AC CHARACTERISTICS

Parameter	Sym	Min	Typ	Max	Units	Conditions
SCL Clock Frequency	f_{SCL}	0	—	100	kHz	
The LOW Period of the Clock	t_{LOW}	4.7	—	—	µs	
The HIGH Period of the Clock	t_{HIGH}	4.0	—	—	µs	
SDA and SCL Rise Time	t_R	—	—	1	µs	
SDA and SCL Fall Time	t_F	—	—	300	µs	
START condition Hold Time. After this period the first clock pulse is generated.	$t_{HD;STA}$	4.0	—	—	µs	
Setup Time for Start Condition (Only relevant for a repeated start condition)	$t_{SU;STA}$	4.7	—	—	µs	
Data Setup Time	$t_{SU;DAT}$	250	—	—	ns	
Data Hold Time for I²C Devices	$t_{HD;DAT}$	0	—	—	µs	See note 2
STOP Condition Setup Time	$t_{SU;STO}$	4.7	—	—	µs	
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	—	—	µs	
Erase/Write Cycle Time (per word)	$T_{E/W}$	20	30	100	ms	C=2500pf, R=10K
Endurance (Number of erase/write cycles)	$N_{E/W}$	—	—	10,000	E/Wcycles	Per byte
Data Retention Time	T_S	10	—	—	years	
Input Capacitance on SCL, SDA	C_I	—	—	7	pf	
Noise Suppression Time Constant at SCL and SDA input	T_I	0.25	0.5	1.0	µs	

NOTES: (1) All values referred to V_{IH} and V_{IL} levels.
(2) Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300ns) of the falling edge of SCL.

FUNCTIONAL DESCRIPTION

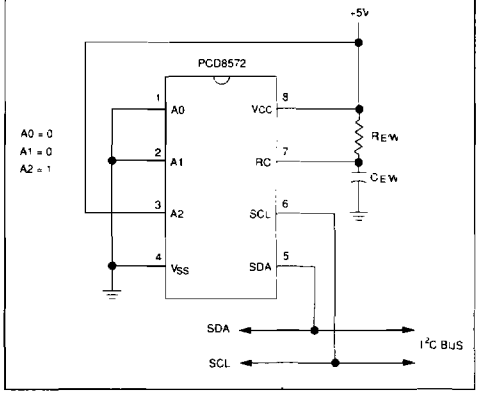
I²C Bus Interface

Figure 1 below shows the typical manner in which the PCD8572 is interfaced to the I²C bus. For purposes of illustration chip address A2,A1, A0 = 100 is shown. This is only one of eight possible addresses since up to eight PCD8572s can be connected to the I²C bus of a single system. The erase/write cycle time of this device $T_{E/W}$ is determined by an external resistor and capacitor: $R_{E/W}$ and $C_{E/W}$.

NOTE:

When the PCD8572 is not used in an 1²C bus configuration, pull-up resistors for SDA and SCL are required.

FIGURE 1 - TYPICAL INTERFACE



Characteristics of the I²C Bus

The I²C bus is intended for communication between different ICs. This serial bus consists of two bi-directional lines: one for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

BUS NOT BUSY

Both data and clock lines remain HIGH.

START DATA TRANSFER

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines the START condition.

STOP DATA TRANSFER

A change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

DATA VALID

The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE + WRITE mode and is not limited in the READ mode. The information is transmitted bytewise and each receiver acknowledges with a ninth bit of which must be provided by the user.

Within the I²C bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCD8572 works in both modes. By definition a device that gives out a message is called "transmitter", the receiving device that controls the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

ACKNOWLEDGE

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that had been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse. Of course setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 2A - DATA TRANSFER SEQUENCE ON THE SERIAL BUS

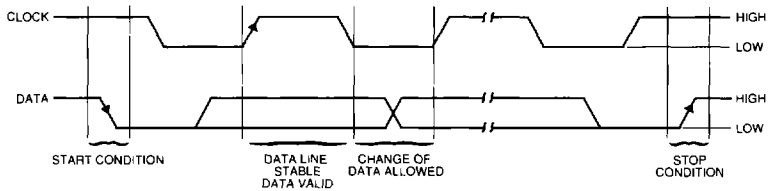
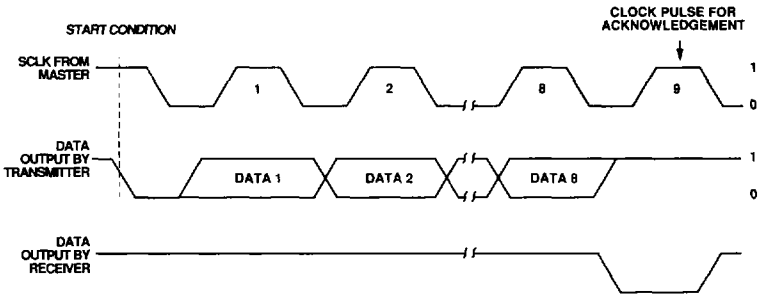
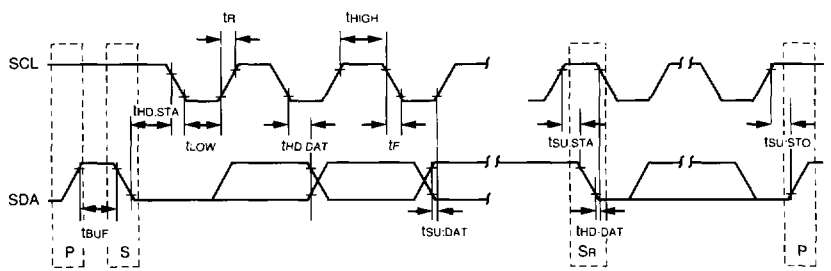


FIGURE 2B - ACKNOWLEDGEMENT



ACKNOWLEDGEMENT: An extra clock pulse is generated during which the receiver pulls the data line LOW.

FIGURE 2C - BUS TIMING REQUIREMENTS



S = START, P = STOP

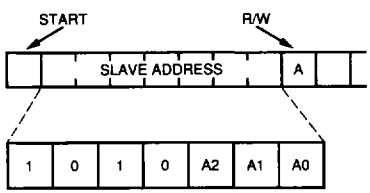
I²C Bus Protocol

A thorough description of the inter-IC bus specification appears in the Philips document number TVE 81107 which is available upon request from Microchip Technology. The following is a condensed description of each mode of operation.

CHIP ADDRESS (SLAVE ADDRESS) ALLOCATION

The three chip address inputs of each PCD8572 (A2, A1, A0) must be externally connected to either +5V (Vcc) of ground (Vss) thereby assigning to each PCD8572 a unique three-bit chip address. Up to eight PCD8572s may be connected to the I²C bus. Chip selection is then accomplished through software by setting the least significant three bits of the slave address to the corresponding hard-wired logic levels of the selected PCD8572. The correct bus protocol shown in Figure 3.

FIGURE 3 - SLAVE ADDRESS ALLOCATION



ERASE/WRITE MODE

In this mode the master transmitter transmits to the PCD8572 slave receiver. Bus protocol is shown in Figure 4. Following the START condition and slave address a logic 0 (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address AN will follow and is to be written to the on-chip address pointer. The data word to be written to the nonvolatile memory is strobed in next, and is loaded in the address pointer. A second data byte may be strobed in following this the address pointer. In the erase/write mode no more than two successive data bytes may be strobed into the PCD8572. The PCD8572 slave receiver will send an acknowledge bit to the master transmitter after it has received the slave address and again after it has received the word address and each data byte. After the STOP condition the erase/write cycle starts. Its duration is approximately 20ms. if only one byte is written, and 40ms. if two bytes are written.

READ MODE

In this mode the master reads the PCD8572 slave after setting the slave address. See Figure 5. Following the write mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address AN is written to the on-chip address pointer. Next, the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the *master receiver and the PCD8572 slave receiver* becomes the slave transmitter. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The PCD8572 slave transmitter will now place the data byte at address AN+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to AN+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the PCD8572 slave without first writing to the (Volatile) address pointer. The first address that is read is the last one stored in the pointer. See Figure 6.

FIGURE 4 - ERASE + WRITE MODE

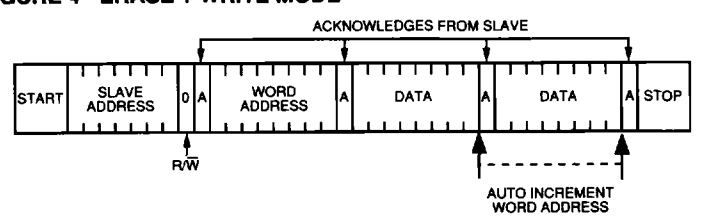


FIGURE 5 - READ MODE

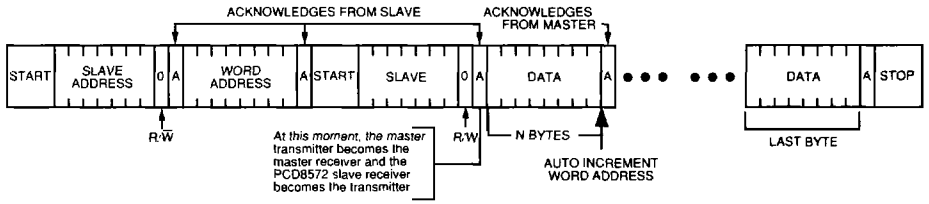
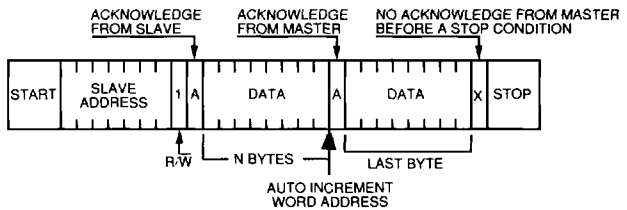


FIGURE 6 - ALTERNATE READ MODE



SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS